Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1 (currently amended). A semiconductor field-effect device structure comprising:

a host structure further comprising a channel region; and

an engineered array of at least one impurity disposed at the channel region of the host structure such that a position of each component atom of the engineered array is ~~substantially~~ fixed by ~~substantially controlled placement~~ atomic scale position control in order to provide substantial control of carrier flow.

2 (original). The field-effect device structure of claim 1 further comprising:

a source region;

a drain region;

a first insulator disposed atop the source region, the drain region, the channel region, and the engineered array; and

a gate disposed atop the first insulator so that a field-effect transistor is formed from the semiconductor field-effect device structure.

3 (original). The semiconductor field-effect device structure of claim 2 wherein the semiconductor field-effect device structure is comprised primarily of silicon, and further comprising a second insulator disposed beneath the semiconductor field-effect device structure to form a silicon-on-insulator field-effect device.

4 (original). The field-effect device structure of claim 1 wherein the engineered array further comprises at least some of the component atoms arranged substantially in at least one row.

5 (original). The field-effect device structure of claim 4 wherein the at least one row comprises a plurality of rows.

6 (original). The field-effect device structure of claim 1 wherein the engineered array further comprises at least some of the component atoms arranged in a substantially ordered pattern resulting at least in part from self-assembly.

7 (original). The field-effect device structure of claim 2 wherein the engineered array further comprises at least some of the component atoms arranged substantially in at least one row.

8 (original). The field-effect device structure of claim 7 wherein the at least one row comprises a plurality of rows.

9 (original). The field-effect device structure of claim 2 wherein the engineered array further comprises at least some of the component atoms arranged in a substantially ordered pattern resulting at least in part from self-assembly.

10 (original). The field-effect device structure of claim 8 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

11 (original). The field-effect device structure of claim 1 wherein the component atoms comprise p-type dopants.

12 (original). The field-effect device structure of claim 1 wherein the component atoms comprise n-type dopants.

13 (original). The field-effect device structure of claim 1 wherein the component atoms comprise p-type dopants and n-type dopants.

14 (original). The field-effect device structure of claim 2 wherein the component atoms comprise p-type dopants.

15 (original). The field-effect device structure of claim 2 wherein the component atoms comprise n-type dopants.

16 (original). The field-effect device structure of claim 2 wherein the component atoms comprises p-type dopants and n-type dopants.

17 (original). A supermolecular structure comprising a host structure and an engineered array of at least one dopant atom disposed at a channel region of the host structure to impart substantial control of a source-drain carrier flow, the supermolecular structure also being described by the formula:

$$H_i Y_{1_j} \ldots Y_{k_l}$$

wherein:

H defines the channel region material;

i is a total number of host matrix atoms;

Y defines the dopant atom type, with 1 to k dopant atom types;

j is the discrete number of dopant atoms of the 1^{st} dopant atom type in the engineered array; and

l is the discrete number of dopant atoms of the k^{th} dopant atom type in the engineered array.

18 (original). The supermolecular structure of claim 17 wherein the engineered array further comprises at least some of the at least one atom arranged substantially in at least one row.

19 (original). The supermolecular structure of claim 18 wherein the at least one row comprises a plurality of rows.

20 (previously presented). The supermolecular structure of claim 17 wherein the engineered array further comprises a substantially ordered pattern of at least some of the at least one dopant atom, the substantially ordered pattern resulting at least in part from self-assembly.

21 (original). The supermolecular structure of claim 19 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

22 (original). A field-effect transistor comprising:

a source region;

a drain region;

a gate structure;

a first insulator disposed beneath the gate structure and above the source region and the drain region; and

a supermolecular structure disposed beneath the first insulator, the supermolecular structure comprising a host structure and an engineered array of at least one dopant atom disposed at a channel region of the host structure to facilitate substantial control of a source-drain carrier flow, the supermolecular structure also being described by the formula:

$$H_i Y_{1_j} \ldots Y_{k_l}$$

wherein:

H defines the channel region material;

i is a total number of host matrix atoms;

Y defines the dopant atom type, with 1 to k dopant atom types;

j is the discrete number of dopant atoms of the 1^{st} dopant atom type in the engineered array; and

l is the discrete number of dopant atoms of the k^{th} dopant atom type in the engineered array.

23 (original). The field-effect transistor of claim 22 further comprising a second insulator disposed beneath the supermolecular structure so that a silicon-on-insulator (SOI) field-effect transistor is formed.

24 (original). The field-effect transistor of claim 22 wherein the engineered array further comprises at least some of the at least one dopant atom arranged substantially in at least one row.

25 (original). The field-effect transistor of claim 24 wherein the at least one row comprises a plurality of rows.

26 (original). The field-effect transistor of claim 22 wherein the engineered array further comprises at least some of the at least one dopant atom arranged in a substantially ordered pattern resulting at least in part from self-assembly.

27 (original). The field-effect transistor of claim 23 wherein the engineered array further comprises at least some of the at least one dopant atom arranged substantially in at least one row.

28 (original). The field-effect transistor of claim 27 wherein the at least one row comprises a plurality of rows.

29 (original). The field-effect transistor of claim 23 wherein the engineered array further comprises at least some of the at least one dopant atom arranged in a substantially ordered pattern resulting at least in part from self-assembly.

30 (original). The field-effect transistor of claim 25 wherein the plurality rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

31 (original). The field-effect transistor of claim 28 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

32-38 (cancelled).